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10/590,225	05/04/2007	Kengo Maeda	559502005500	6947

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EXAMINER	
ROJAS, DANIEL E	
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2816	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/590,225	MAEDA ET AL.	
	Examiner	Art Unit	
	DANIEL ROJAS	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 May 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *5* is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 May 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *4/11/2007*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuzaki et al (US Patent No. 6,088,255) in view of Kondo (US Patent No. 6,417,706).

4. For claim 1, Matsuzaki teaches (in Figure 11) a DLL circuit having a dummy delay (280 and 290, as explained below) corresponding to delay between an internal clock delay (280, which is equal to the delay generated by input buffer 800) and an external clock (output of 290 which is equal to the output of 900, as explained below), a variable delay addition circuit (210 and 220) for adjusting delay amount according to a delay amount adjustment signal (output of 400), and a phase comparison circuit (300 and 400) for comparing a phase of the internal clock (output of 800) with a phase of a delay clock input via the variable delay addition circuit (220) and the dummy delay (280

and 290) and outputting the delay amount adjustment signal (400) to the variable delay addition circuit, the DLL circuit comprising: a means for inputting a first signal set at a logic "1" during 1 clock cycle of the internal clock to the variable delay addition circuit via the dummy delay as an initialization mode at a start of burst (inherent based on the structure of Matsuzaki's Figure 11); a means for detecting duration time of the logic "1" of the first signal input (300 and 400) by the variable delay addition circuit through the dummy delay until the end of the 1 clock cycle of the internal clock and setting an initial value of delay amount of the variable delay addition circuit by setting the delay amount of the variable delay circuit in the variable delay addition circuit based on the duration time as the initialization mode at the start of burst (inherent based on the structure of Matsuzaki's Figure 11); but fails to teach that the variable delay addition circuit has a coarse delay circuit and a fine delay circuit. Matsuzaki's specification teaches that both the dummy-input buffer 280 and the dummy-data-output buffer 290 have a delay value (column 25, lines 47-49), that the dummy-input buffer 280 has the same delay as the input buffer 800, and that the dummy-data-output buffer 290 has the same delay as the data-output buffer 900 (column 16, lines 1-9). Kondo teaches a delay locked loop having a coarse and fine delay as a variable delay circuit. It would have been obvious to one of ordinary skill in the art at the time of invention to use a variable delay addition circuit comprising a coarse and a fine delay circuit for Matsuzaki's first and second variable delay circuits since the application of a known technique (i.e. the use of a coarse and fine delay circuit as a variable delay circuit) to a known device (i.e. variable delay circuit) has been recognized as part of the ordinary capabilities of one having

ordinary skill in the art. The modified version of Matsuzaki with the teachings of Kondo as defined above teaches a clock output means (900) for generating an output clock that synchronizes with the external clock one clock cycle behind with the internal clock (as explained below) delayed by the coarse delay circuit and the fine delay circuit in the variable delay addition circuit (inherent based on the structure of Matsuzaki's Figure 11) and with the delay amount of the coarse delay circuit and the fine delay circuit in the variable delay addition circuit corrected according to the delay amount adjustment signal (inherent based on the structure of Matsuzaki's Figure 11) output from the phase comparison circuit as a lock mode after initial setting of the delay amount in the variable delay addition circuit (inherent based on the structure of Matsuzaki's Figure 11 since upon initialization of a delay circuit, it is inherent that the Matsuzaki's variable delay addition circuit will have an initial value) and a means for setting an initial value of delay amount of the variable delay addition circuit by setting the delay amount of the coarse delay circuit in the variable delay addition circuit based on the duration time as the initialization mode at the start of burst (inherent based on the structure). Matsuzaki teaches in his specification that "the delay-control circuit 400 controls the delay amount of the first variable delay circuit 210 and the second variable-delay circuit 220 such that a phase difference between the external clock signal CLK and the internal clock signal becomes equivalent to a predetermined number of clock [cycles] such as one clock cycle" (column 16, lines 17-22).

5. For claim 2, the modification of Matsuzaki with Kondo as defined above teaches a DLL circuit (Figure 11, Matsuzaki) having a dummy delay (280 and 290)

corresponding to delay between an internal clock delay (280, which is equal to the delay generated by 800) and an external clock (output of 290 which is equal to the delay generated by 900), a variable addition circuit having a coarse delay circuit and a fine delay circuit (210 and 220, as explained above), for adjusting delay amount according to a delay amount adjustment signal (output of 400), and a phase comparison circuit (300 and 400) for comparing a phase of the internal clock (output of 800) with a phase of a delay clock input via the variable delay addition circuit (220) and the dummy delay (280 and 290) and outputting the delay amount adjustment signal to the variable delay addition circuit (as shown in Figure 11), the DLL circuit comprising: a means for inputting a first signal set at a logic "1" during 1 clock cycle of the internal clock to the variable delay addition circuit via the dummy delay as an initialization mode at a start of burst (inherent based on the structure of Matsuzaki's Figure 11); a means for detecting duration time of the logic "1" of the first signal input (300 and 400) by the variable delay addition circuit through the dummy delay until the end of the 1 clock cycle of the internal clock and setting an initial value of delay amount of the variable delay addition circuit by setting the delay amount of the coarse delay circuit in the variable delay addition circuit based on the duration time as the initialization mode at the start of burst (inherent based on the structure of Matsuzaki's Figure 11); and a clock output means (900) for generating an output clock (OUT) that synchronizes with the external clock one clock cycle behind with the internal clock delayed by the coarse delay circuit and the fine delay circuit in the variable delay addition circuit and with the delay amount of the coarse delay circuit and the fine delay circuit in the variable delay addition circuit

corrected according to the delay amount adjustment signal (inherent based on the structure of Figure 11 as modified by Kondo) output from the phase comparison circuit as a lock mode after initial setting of the delay amount in the variable delay addition circuit (any delay circuit inherently has an initial setting), wherein the coarse delay circuit operates as the variable delay addition circuit and a means for storing setting of the initial value in the initialization mode (inherent based on the structure of Figure 11) and operates as a coarse variable delay addition circuit having coarse unit delay amount (inherent to any variable coarse delay circuit) in the lock mode (lock mode being the operation mode), and the fine delay circuit operates as a fine variable delay addition circuit (inherent to any fine delay circuit) adding delay amount for complementing the unit delay amount of the coarse delay circuit by having fine unit delay amount in the lock mode (inherent when in an operating mode). Matsuzaki's specification teaches that both the dummy-input buffer 280 and the dummy-data-output buffer 290 have a delay value (column 25, lines 47-49), that the dummy-input buffer 280 has the same delay as the input buffer 800, and that the dummy-data-output buffer 290 has the same delay as the data-output buffer 900 (column 16, lines 1-9). Matsuzaki also teaches in his specification that "the delay-control circuit 400 controls the delay amount of the first variable delay circuit 210 and the second variable-delay circuit 220 such that a phase difference between the external clock signal CLK and the internal clock signal becomes equivalent to a predetermined number of clock [cycles] such as one clock cycle" (column 16, lines 17-22).

6. For claim 3, Matsuzaki further teaches a means for preventing delay from being added to the delay clock in the fine delay circuit in the variable delay circuit, when the phase of the delay clock obtained by adding predetermined threshold delay amount (280 and 290) to the internal clock lags behind the internal clock, as a determination result of the phase comparison circuit (inherent to the operation of the phase detector 300 in Matsuzaki's Figure 11) in the lock mode (i.e. operational mode).

7. For claim 4, examiner takes official notice that delay elements with a constant delay time are notoriously old and well known to comprise an even number of inverters wherein the inverter comprises a PMOS transistor with its source connected to a positive power supply and its drain connected to the output, an NMOS transistor wherein the source is connected to ground or a low potential and the drain is connected to the output, and that both said NMOS and PMOS transistors have a gate connected to an input signal. Kondo teaches the details of his coarse delay line in Figure 2 and the details of his fine delay line in Figure 3. The coarse delay line of Figure 2 comprises a plurality of delay elements in series but is silent as to the details of the delay elements. Therefore, each one of the delay elements (411) can be made up of an even number of inverters since the use of a known technique (using an even number of inverters as a buffer) to a known device (delay element with a constant delay time) has been recognized as a part of the ordinary capabilities of one skilled in the art. As shown in Figure 3, the fine delay line comprises a plurality of inverters. Since both the coarse and fine delay lines comprise at least two inverters in series, when input signal to the first inverter is low, the first inverter connects the positive power supply to the output via

the PMOS transistor. The output of the first PMOS transistor is inputted to the input of the second inverter, wherein the second inverter connects ground or the low potential power supply to the output. Therefore, the first inverter (i.e. an inverter circuit) has a positive characteristic in regard to the power supply voltage and the second inverter (i.e. a circuit) has a negative characteristic in regard to the power supply voltage (i.e. the opposite characteristic of the inverter circuit).

Allowable Subject Matter

8. Claim 5 is allowed.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DANIEL ROJAS whose telephone number is (571)270-5070. The examiner can normally be reached on Monday-Friday 7:30-8 EST, alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Drew Richards can be reached on 571-272-1736. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Tuan T. Lam/
Primary Examiner, Art Unit 2816

/D. R./
Examiner, Art Unit 2816